REMARKS

As an initial matter, the Examiner has objected to the Inventor's Declaration filed on March 14, 2002. The Examiner asserts that there are "underlines and other markings on the signature page" (Office Action dated December 2, 2004, at 2, lines 12-14. Applicant disagrees and files herewith a photocopy of the Japanese Language "Declaration and Power of Attorney for Patent Application" (PTO/SB106) executed on March 11, 2002 by Shinji Furusho. There are no extraneous markings on this Declaration.

The Abstract and Title of the Invention have been amended and now comply with all requirements of the United States Patent and Trademark Office (USPTO).

Claims 1-10 have been amended and new claims 12 and 13 have been added. More specifically, claim 1 has been amended so the preamble recites "A computer system having architecture of a parallel computer" as supported on page 8, line 20, to page 9, line 2, of the specification as originally filed. Claims 2-8 depend either directly, or indirectly, on claim 1 and have been amended in accordance with this amendment to claim 1. This amendment has no limiting affect on the scope of these claims.

Claim 1 has also been amended to improve grammar and punctuation, which also has no limiting affect on the scope of claim 1. The phrase "and/or" has been replaced with its usual meaning of (a), or (b), or (a) and (b). Claims 2, 3, 4, 5, 7, 8, 9 and 10 have also been amended to improve grammar and punctuation. No claim has been narrowed in view of any reason for patentability.

Claim 9 has been additionally amended to recite that it has "architecture of a parallel computer" as supported by claim 1.

New claim 12 depends on claim 1 and new claim 13 depends on claim 9. Claims 12 and 13 each recited that "the plurality of sets of buses are connected in parallel to the CPU module and to each memory module" as supported by Figure 1 of the application as originally filed.

No new matter has been added by the above amendments.

The Invention

The presently claimed invention pertains broadly to apparatuses having parallel computing architecture, such as is used to implement a Single Instruction Stream, Multiple Data Stream ("SIMD") architecture for performing general purpose parallel processing using appropriate and high-speed memory control. More specifically, the present invention pertains to a computer system having architecture of a parallel computer, wherein the computer system has all of the features recited in claim 1 of the present application. In addition, the present invention also pertains to an information processing unit having all of the features recited in claim 9 of the present application.

Various other embodiments, in accordance with the present invention, are recited in the dependent claims. All of the various embodiments, in accordance with the present invention, advantageously utilize an architecture of a parallel computer so that parallel processing by means of appropriate and high-speed memory control can be achieved.

The Rejections

Claims 1-8 stand rejected under 35 U.S.C. § 101 for being directed to non-statutory subject matter. Claims 1-11 also stand rejected under 35 U.S.C. § 112, second paragraph, as indefinite.

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Thiel (European Document EP 0 408 810 A1) in view of Hennessy (Computer Organization and Design, at 16-81, 541 and 712-713.

Applicant respectfully traverses the rejection and requests reconsideration of the instant claims for the following reasons.

Applicant's Arguments

In view of the present amendment, claims 1-8 now pertain to a "computer system having architecture of a parallel computer," which is statutory subject matter under 35 U.S.C. § 101. In addition, claims 1-13 are now in full compliance with 35 U.S.C. § 112.

The Section 103 Rejection

A patentability analysis under 35 U.S.C. § 103 requires (a) determining the scope and content of the prior art, (b) ascertaining the differences between the prior art and the claimed subject matter, (c) resolving the level of ordinary skill in the pertinent art, and (d) considering secondary considerations that may serve as indicia of nonobviousness or obviousness. Graham v. John Deere Co. of Kansas City, 148 U.S.P.Q. 459, 467 (1966). Furthermore, a proper rejection under Section 103 further requires showing (1) that the prior art would have suggested to a person of ordinary skill in the art that they should make the claimed device or carry out the claimed process, (2) that the prior art would have revealed to a person of ordinary skill in the art that in so making or doing, there would have been a reasonable expectation of success, and (3) both the suggestion and the reasonable expectation of success must be found in the prior art and not in the applicants' disclosure. In re Vaeck, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991).

In the present case, the Examiner's rejection of the instant claims 1-11 under 35 U.S.C. § 103 is clearly untenable because the scope and content of the prior art fails to teach all of the claimed subject matter.

The Thiel Document

European Publication EP 0 408 810 A1 to Thiel (hereafter, the "Thiel Document") teaches a multi-processor computer system that includes sixteen data processors (32a,.., 32p), each connected to a single communication bus (36), (See Abstract, and Figure 5). The communication bus (36) includes a data bus (40) for carrying data and an address bus (38) for carrying associated labeling information uniquely identifying the data (See Abstract). Each processor (32) includes read and write detectors (52) connected to the address bus (38) for detecting labeling information for data required by, or presently stored in, the respective processor (32), (See Abstract). A bulk memory (44) having read and write detectors (46) is connected to the communication bus (36) and an address generator (42) supplies labeling addresses to the address bus (38), (See Abstract).

The Thiel Document teaches that, for each address, one processor (32) or the bulk memory (44) supplies the corresponding data to the data bus (40), and other

processors and/or the bulk memory requiring the data read the data from the data bus (40), (See Abstract). In this way, data is transferred between processors and/or the bulk memory wherein the address bus (38) and the read and write decoders (52), (46) are configured for multi-dimensional addressing.

No Architecture of a Parallel Computer

A person of ordinary skill in the art would immediately recognize that the Thiel Document teaches a computer system configured for multi-dimensional addressing, but not a "computer system having architecture of a parallel computer" as recited in claim 1. Likewise, the Thiel Document does not teach, or even suggest, "architecture of a parallel computer" is constituted such that (i) "a series of data having a stipulated relationship is given a space ID," and (ii) "the processor of each memory module manages a table that contains at least said space ID, the logical address of a portion of the series of data managed, the size of said portion and the size of the series of data" as recited in claims 1 and 9. In particular, the Thiel Document is limited to teaching a multi-processor computer system that is designed to minimize time consuming data transfers between the distributed local memories of the processors when processing multi-dimensional data arrays. The device of the Thiel Document achieves this objective by using a Multi-Dimensional (MD) Address Generator that is capable of structuring multi-dimensional addresses of data arrays in a compact way for storage in linearly addressed memories.

As shown in Figure 5 of Thiel, the computer system (30) includes a control processor (56), the MD Address Generator (42) and the plurality of processors (32a), (32b), (32p), wherein each processor has a CPU (48a), (48b), (48p), a local memory (50a), (50b), (50p), and a multi-dimensional (MD) Decoder and Address Generator (52a), (52b), (52p). The computer system (30) also includes a control bus (54) connecting the control processor (56) to the MD Address Generator (42) and the plurality of CPUs (48a), (48b), (48p), a MD Parallel Address Bus (38) connecting the MD Address Generator (42) to the plurality of MD Decoders and Memory Address Generators (52a), (52b), (52p) of the processors (32a), (32b), (32p), respectively, and a 64 bit wide data bus (40) for transferring data between local memories (50a), (50b), (50p) and the processors (32a), (32b), (32p), respectively.

As shown in Figure 8 of Thiel, the MD Address Decoder (52) includes N one-dimensional linear decoders (100a), (100b), etc., connected to the MD Address Bus (38). The shift and mask network (104) extracts only certain bits from the MD Address Bus (38) depending on the value held in the value register (103), and shifts the extracted bits down in significance depending on the value held in the shift value registers (106). The output of the shift and mask network (104) is fed to a linear address generator (130) for generating a local memory location address from a decoded MD address.

From the linear address generator (130), the address of a given decoded address is shown in the following form:

$$\text{Address} = BP + (Aa \times Da) + (Ab + Db) + \ldots..$$

where BP is the array base address, Aa, Ab,...are the values of the decoded field addresses for the dimension zero, dimension one, etc., and Da, Db,...are the values stored in the dimension zero field increment register (134a), dimension one field register (134b), etc. (See col. 6, line 55, to col. 7, line 7).

A person of ordinary skill in the art would realize from the above description that the Thiel Document does not teach that "the processor of each memory module manages a table that contains at least said space ID, the logical address of a portion of the series of data managed, the size of said portion and the size of the series of data" as recited in claims 1 and 9. Assuming, *arguendo*, that the registers (112), (114), (118), (120) of decoders (100a), (100b), etc. and the registers (140), (142) of the address generators (52) may reasonably be construed to define a "table" as recited in claims 1 and 9 of the present application, the content of such a "table" taught by Thiel would be completely different from the content of the "table" recited in the present claims.

For instance, the contents of the registers (112), (114), (118), (120), (140), (142) are upper and lower boundary values of an N+1 dimensional address array, which cannot be reasonably construed to be addresses and size of series of data. Rather, the contents of the registers (112), (114), (118), (120), (140), (142), which pertain to various upper and lower boundaries of an N+1 dimensional address array, plainly do not disclose a "table" having entries for (i) "space ID," (ii) "the logical address of a portion of the series of data managed," (iii) "the size of said portion," and (iv) "the size of the series of data" as recited in claims 1 and 9 of the present application.

As discussed above, the Thiel Document does not reasonably teach, or even suggest, a "table" that contains a "space ID" in accordance with the present invention. By storing the space ID in the table, it becomes advantageously possible to generate and delete space Ids depending on the structure of the data that is to be stored or processed (See, for example, Figures 3 and 4 of the present application). This capability eliminates garbage collection and optimizes the use of memory for data series of various dimensionality (See, for example, page 10, line 23, to page 11, line 4, of the present specification).

As discussed above, the Thiel Document does not reasonably teach, or even suggest, a "table" that contains the logical address or size of the portion of the series of data that is managed. As stated previously, the content of the registers (112), (114), (118), (120) of the decoders (100a), (100b), etc. includes numbers that refer to boundaries of address arrays, which are not reasonably interpretable to be logical addresses of data. For the same reason, the Thiel Document does not teach a "table" that contains the "size of the series of data" as recited in claims 1 and 9 of the present application.

The Thiel Document also clearly does not teach, or even suggest, "wherein the plurality of sets of buses are connected in parallel to the CPU module and to each memory module" as recited in new claims 12 and 13.

No Plurality of Sets of Buses

A person of ordinary skill in the art would also immediately recognize that the Thiel Document does not teach, or even suggest, a "plurality of sets of buses that make connections between the CPU module and memory modules" as recited in claim 1 and 9. Specifically, the Thiel Document teaches a single communication bus (36) that makes communications between the local memory of the processors (32a), (32b), (32p) and the bulk memory (44) as shown in Figure 5. The communication bus (36) is a single bus constructed to include component buses, such as data bus (40) and address bus (38). However, communication bus (36) is not connected to make communications with the control processor (56) or the CPUs of the processors (32a), (32b), (32p) as shown in Figure 5. Therefore, communication bus (36) cannot be reasonably construed

to be a "plurality of sets of buses that make connections between the CPU module and memory modules" in accordance with the presently claimed invention.

A "control bus," as shown in Figure 5 of the Thiel Document, is provided to make connections between the control processor (56), the bulk memory (44) and the processors (32a), (32b), (32p), but this is only a single bus. Assuming, *arguendo*, that the communication bus (36) and the control bus (See Fig. 5) taught by the Thiel Document may be construed as a "set of buses" making communications between the control processor (56) and the local memories of the processors (32a), (32b), (32p), then Thiel still plainly fails to teach, or even suggest, a "plurality of sets of buses that make connections between the CPU module and memory modules" as recited in claims 1 and 9.

A person of ordinary skill in the art of parallel computing processing would know that bus communication between processors requires the following functionalities: (a) addressing a processor, (b) receiving/transferring data from/to the addressed processor, and (c) receiving/sending instructions from/to the processor. These functionalities are essential to bus communication because, for example, a bus cannot select a processor for data transfer without the addressing functionality, or, for example, data cannot be read by an addressed processor without the instruction sending functionality. Therefore, a person of ordinary skill in the art would immediately recognize that the "control bus," the "data bus" and the "address bus" shown in Figure 5 are the three bus elements (i.e., control, data, and address) that form a single bus.

Examiner's Admissions

However, these are not the only deficiencies of the scope and content of the Thiel Document. As admitted by the Examiner, the Thiel Document teaches that the processors (32) have a CPU and a local memory, by not a "RAM core" as recited in claims 1 and 9 (Office Action, dated December 2, 2004, at 7, lines 3-4, and at 13, lines 16-17). The Examiner also admits that the Thiel Document does not teach, or even suggest, that the memory modules receives a synchronization signal for achieving synchronization with the CPU module and other memory modules in accordance with claim 3 (Office Action, dated December 2, 2004, at 8, lines 12-19).

The Hennessy Reference

The excerpt from "Computer Organization and Design," 2nd Edition, 1998, pp. 16-18, 541 and 712-713, (hereafter, the "Hennessy Reference") teaches that a RAM can be used as the local memory in a memory hierarchy of a computer in place of a sequential access memory, and that processors operating in parallel need to cooperate when operating on shared data, which is achieved by synchronization.

It is evident that the Hennessy Reference is used to establish a narrow premise, and that the Hennessy Reference does not teach, or even suggest, (1) an "architecture of a parallel computer" is constituted such that (i) "a series of data having a stipulated relationship is given a space ID," and (ii) "the processor of each memory module manages a table that contains at least said space ID, the logical address of a portion of the series of data managed, the size of said portion and the size of the series of data" as recited in claims 1 and 9, (2) a "plurality of sets of buses that make connections between the CPU module and memory modules" as recited in claims 1 and 9, and (3) "wherein the plurality of sets of buses are connected in parallel to the CPU module and to each memory module" as recited in new claims 12 and 13.

Summary of the Scope and Content of the Prior Art

Neither the Thiel Document, nor the Hennessy Reference, teach or suggest a computing system, or an information processing unit, wherein (1) an "architecture of a parallel computer" is constituted such that (i) "a series of data having a stipulated relationship is given a space ID," and (ii) "the processor of each memory module manages a table that contains at least said space ID, the logical address of a portion of the series of data managed, the size of said portion and the size of the series of data" as recited in claims 1 and 9, (2) a "plurality of sets of buses that make connections between the CPU module and memory modules" as recited in claims 1 and 9, and (3) "wherein the plurality of sets of buses are connected in parallel to the CPU module and to each memory module" as recited in new claims 12 and 13.

Conclusion

Claims 1-13 each recite statutory subject matter in accordance with 35 U.S.C. § 101 and are in full compliance with the requirements of 35 U.S.C. § 112. Furthermore, the rejection under 35 U.S.C. § 103(a) is untenable and should be withdrawn because neither the Thiel document nor the Hennessy Reference reasonably teaches, or even suggests, (1) an "architecture of a parallel computer" is constituted such that (i) "a series of data having a stipulated relationship is given a space ID," and (ii) "the processor of each memory module manages a table that contains at least said space ID, the logical address of a portion of the series of data managed, the size of said portion and the size of the series of data" as recited in claims 1 and 9, (2) a "plurality of sets of buses that make connections between the CPU module and memory modules" as recited in claims 1 and 9, and (3) "wherein the plurality of sets of buses are connected in parallel to the CPU module and to each memory module" as recited in new claims 12 and 13.

For all of the above reasons, claims 1-13 are in condition for allowance and a prompt Notice of Allowance is earnestly solicited.

Questions are welcomed by the below-signed attorney for applicant.

Respectfully submitted,

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